



The Partner For Success

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Signalintegrität und Eigenstörsicherheit elektronischer Baugruppen

ZVEI Initiative „Design Chain“
Siemens AG – München
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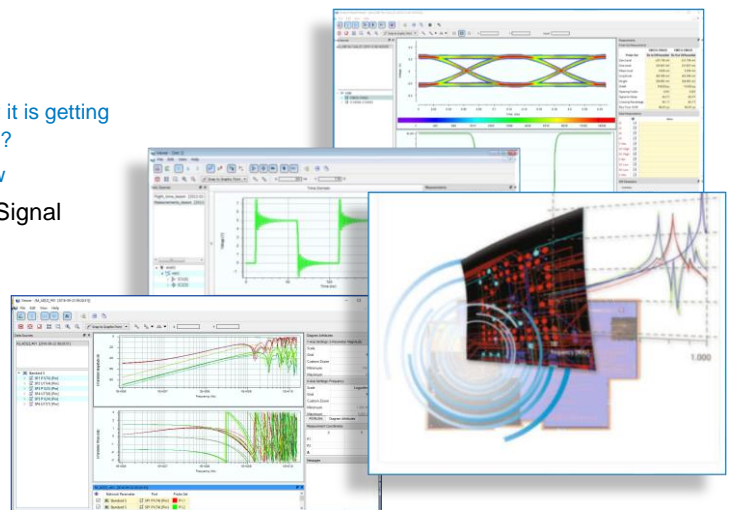
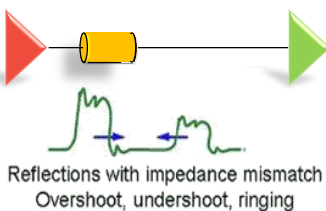


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Signal Integrity for Improved EMI Control - Agenda

- Preface & Motivation
- Introduction
 - Signal-Integrity: What is the problem and why it is getting more and more a problem for PCB Designers?
 - Addressing Signal Integrity – A Brief Overview
- Electronic Product Design with Concurrent Signal Integrity
- Application Samples
- Conclusion, Q & A



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Zuken – Wer wir sind ...

Corporate Summary

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Founded	1976
Revenue Year Ended March 2017	\$231,500,427*
Corporate Headquarters	Yokohama, Japan
European Headquarters	Munich, Germany
North American Headquarters	Westford, Massachusetts
Stock Listing	Tokyo Stock Exchange Level-1
Employees	1,290
Operational Excellence	Profitable, no debt

* using the original currency and the average exchange rate for the period.

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Zuken Lösungen zur Elektronikentwicklung

CR-8000™ System Level 2D/3D Multiboard Design

The image displays a collection of Zuken software tools used for system-level 2D/3D multiboard design. The tools shown include Design Gateway, GPM, Circuit DR Navi, EMC Adviser, Design Force, DS CR, System Planner, Board Viewer, DFM Center, and DRAGON. The central focus is a large, detailed circuit board design with various components and traces.

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Zuken: Engineering-Driven Organization

■ Six Development Centers

R&D Headquarters:	Yokohama, Japan
SI and EMC R&D:	Paderborn, Germany
R&D and Support:	Ulm, Germany
R&D Automotive:	Erlangen, Germany
R&D:	Bristol, United Kingdom
R&D:	San Jose, California, USA

■ Development Engineers

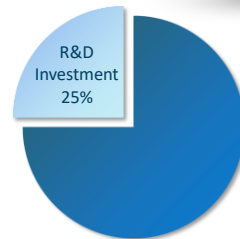
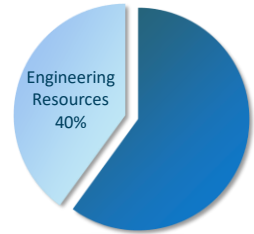
Worldwide staffing:	325
Average Tenure:	12 years

■ Service and Support Engineers

Worldwide staffing:	400
Average Tenure:	11 years

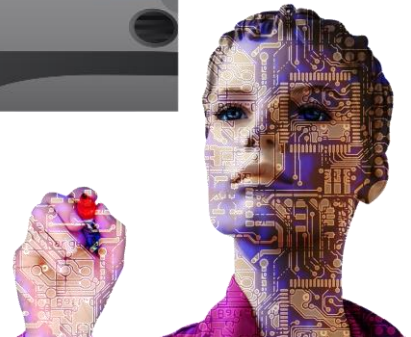
■ 25% R&D investment per year

To relate: VW Group in 2017 ≈ 7%, Tesla in 2018 ≈ 8%,
Intel 2018 close to 20% (Sources: Statistica-Web, Yearly reports, Wikipedia etc.)



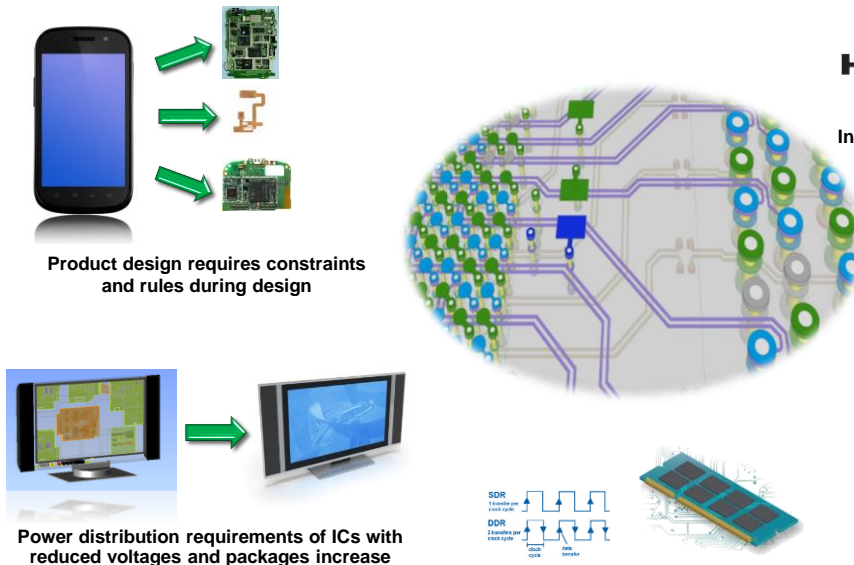
Observation

Electronic and Electrical Systems change our Way of Life

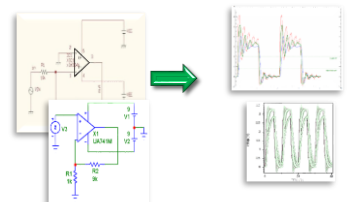


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Todays PCB Design Issues



Increases in data transmission and electrical performance constraints, signal speed



SI analysis often conducted in isolated tools, sometimes requiring additional manual data entry

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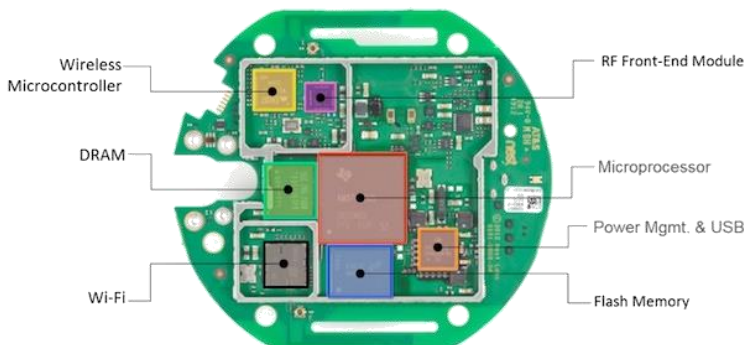
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Example: IoT and IIoT - Tear down of Nest™ Thermostat

Hardware Design Requirements (including Signal Integrity)

- Texas Instruments Sitara Processor (OMAP3 family), 1GHz with ARM Cortex A8
- 512 MB LPDDR, 1.8V (first generation), now LPDDR3 at 1.35V with stringent design (JEDEC = Signal Integrity) requirements
- WiFi, USB (and RF)
- Special form factor, dedicated mechanical requirements
- Flex and rigid boards combine the whole device

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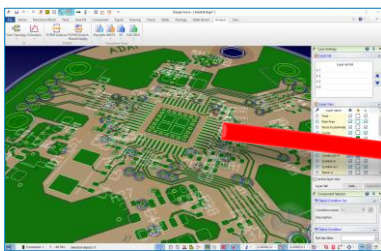
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Signal Integrity is nearly Everywhere

IoT and Signal Integrity

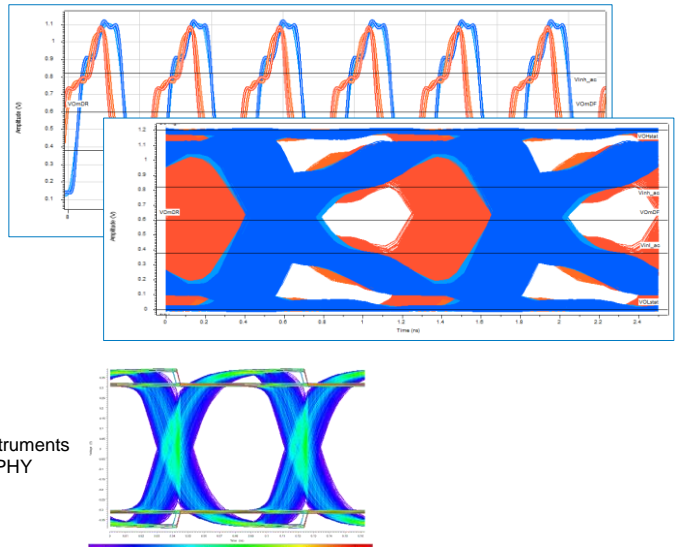
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- ARM core based micro-controllers dominate the market, low power DDR3 memory operates at 1.2V, voltages are further narrowing down, so will the margins do
- Waveform analysis often not sufficient any longer (eye diagram compliance checks)
- Various communication schemes may require SERDES alike protocol analysis



Texas Instruments
USB 3.0 PHY

LP-DDR3 address signal ARM→ Memory @ 400MHz



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Signal Integrity: New Kids on the Block?

Not Really

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Signal integrity
From Wikipedia, the free encyclopedia

Signal integrity or **SI** is a set of measures of the quality of an electrical signal. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform. However, digital signals are fundamentally analog in nature, and all signals are subject to effects such as noise, distortion, and loss. Over short distances and at low bit rates, a simple conductor can transmit this with sufficient fidelity. At high bit rates and over longer distances or through various mediums, various effects can degrade the electrical signal to the point where errors occur and the system or device fails. Signal integrity engineering is the task of analyzing and mitigating these effects. It is an important activity at all levels of electronics packaging and assembly, from internal connections of an integrated circuit (IC),^[1] through the package, the printed circuit board (PCB), the backplane, and inter-system connections.^[2] While there are some common themes at these various levels, there are also practical considerations, in particular the interconnect flight time versus the bit period, that cause substantial differences in the approach to signal integrity for on-chip connections versus chip-to-chip connections.

Some of the main issues of concern for signal integrity are ringing, crosstalk, ground bounce, distortion, signal loss, and power supply noise.

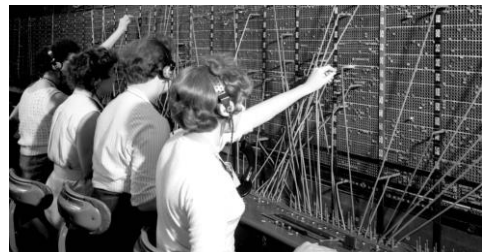
Contents [hide]

- History
- On-chip signal integrity
 - Finding IC signal integrity
 - Fixing IC signal integrity
- On-die termination

Design to the limits

Eigenstörsicherheit:

Fähigkeit eines elektronischen Gerätes, trotz externer Störungen noch zufriedenstellend zu funktionieren (Elektromagnetische Beeinflussbarkeit, EMB)



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The Emerging of Simulation

Simulation = Working on a "Digital Twin"



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Picture: Creative Analytics

Perceived as nightmare...

- Interfaces to host eCAD (often never work)
- Libraries (never complete)
- Models (from where)
- Complex tooling...
- Difficult to explain results...
- Expensive...

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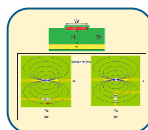
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Signal Integrity (and PCB Design Rules) over the Time

- The early days: Few design rules (e.g. parallel length & spacing) for routing (length, spacings), **impedance** requirements
- In the 1990ies and 2000 years: More complex design rules, EMC regulations, emerging of field solvers and simulation
- Today: Advanced communication channels with high data rates (56GB/s not exotic any more), ultra fast memories, tight design rules may will cause PCB design just based on rules to run out of steam



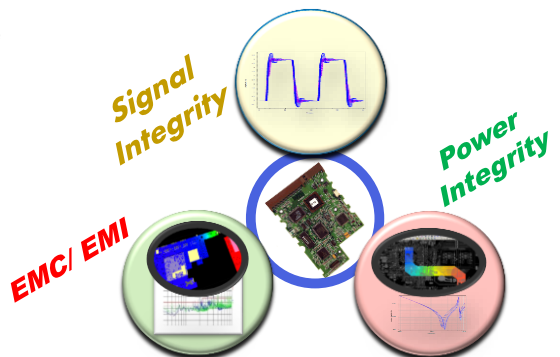
→ virtual prototyping with embedded signal integrity helps here



Impedance Control



CE



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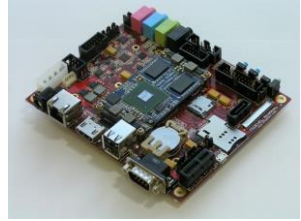
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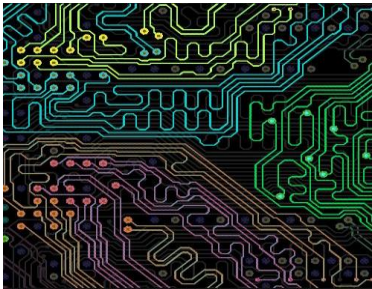
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Reference Designs?

- Its established good design practise to study (and adopt ?) smaller or larger parts of the semiconductor reference designs
- Question: Does this work for complex routing structures/constraints like DDR3/DDR4 and their Signal Integrity behaviour ?
- Answer: Be very careful and keep your heads up!
- To copy the routing structure from the reference design requires a huge amount of trust that your application matches the reference design conditions



Source: iMX6-REX



Source: FEDEVEL

- The number of layers (costs) and selected components like the decoupling capacitors (again, costs) may make your design to be a complete different thing
- Your use of the silicon is never exactly as the IC vendors reference board, which is typically rather large, not cost neither form factor optimized
- **Design instead with Signal (and Power) Integrity in mind**, know the potential culprits and establish dedicated routing rules for these

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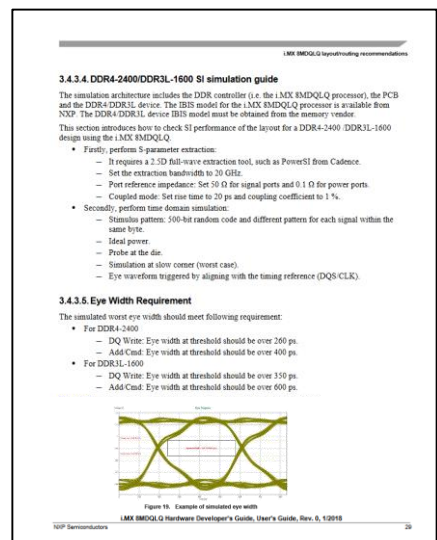
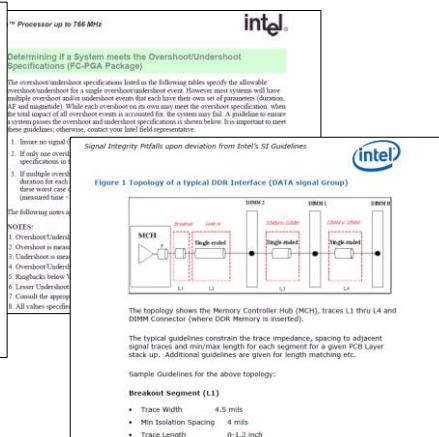
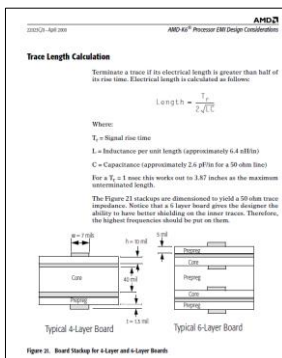
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IC Vendor Guidelines

Intel Yellow Books

- Intel PentiumPro Design guideline sample (issued 1995 under NDA)
- Hardware design guidelines did more and more electrical (!) rules (→ design constraints)



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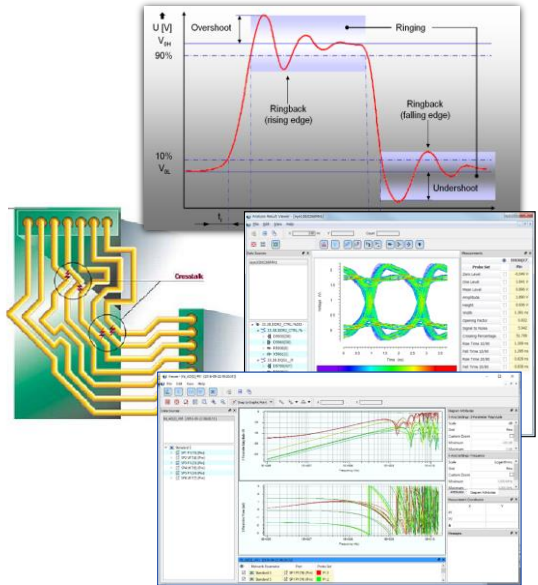
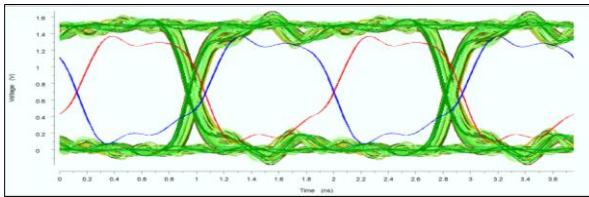
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Glossar of Signal Integrity Problems

A Short tour through the Dungeon

- **Reflection and Ringing** occur on discontinuities or electrical long transmission lines with fast edges, they impact the timing behavior as well
- The cause for **Crosstalk** is the transfer of energy from one electric circuit into another (parallel routing patterns, same layer or layer-to-layer)
- **Insertion loss/return loss** and **impedance** over time characterize the interconnect structure
- Multi-gigabit effects (like **Intersymbol Interference**) are analyzed using eye diagrams. Such diagrams provide figures of merit for **SERDES** channels (BER) as well
- Interconnect timing is often checked by **eye-diagrams** of multiple signals (e.g. DDR data to strobe to clock)



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Impedance Rule Example

DDR3 Design-Guide NXP

NXP Semiconductors
Data Sheet: Technical Data

S32V234 Data Sheet

Features

- ARM® Cortex®-A53, 64-bit CPU
 - Up to 1000 MHz, Quad ARM Cortex-A53
 - 32 KiB/128 KiB L1-L2 Cache
 - NEON™ MPF co-processor
 - Dual precision FPU
 - 2 clusters with 2 CPUs and 256 KiB L2-cache each
 - Memory Management Unit
 - GIC Interrupt Controller
 - ECC parity error support for its memories
 - Generic timers
 - Fault occupation by hardware for redundant executed application software on multiple core cluster
- ARM Cortex-M4, 32-bit CPU
 - Up to 133 MHz
 - 16 KiB/16 KiB L1-L2 Cache
 - 32x32 KiB tightly coupled memory (TCM)
 - ECC parity support for its memories
- Clocks
 - Phase Locked Loops (PLLs)
 - External crystal oscillator (PNOOSC)
 - 1 FRC oscillator
- System protection and power management features
 - Flexible run modes to consume low power based on application needs
 - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
 - Power gating of unused A53 cores and GPU
 - Low and high voltage warning and detect
 - Hardware CRC module to support fast cyclic redundancy checks (CRC)
 - 128-bit unique chip identifier
 - Hardware watchdog
 - eDMA controller with 32 channels with DMA (DMAUX)
 - Extended Resource Domain Controller

S32V234

- Safety concept
 - ISO 26262, ASIL target
 - Measures to detect faults in memory and logic
 - Measures to detect single point and latent faults
 - Quantitative root of content analysis of functional safety (FMEDA) tailored to application specifics
 - Safety manual and FMEDA report available
- Security
 - CSE with 16 KiB of on-chip Secure RAM and ROM
 - ARM TrustZone (TZ) architecture support
 - Boot from NOR flash with AES-128 CTR
 - On-Chip One-Time Programmable element Controller (OCOTP_CTRL) with on-chip electrical fuse array
 - System FTAG Controller (SFC)
- Debug functionality
 - Standard JTAG and Compact JTAG
 - 16-bit Trace port, Serial Wire Output port
- Timers
 - General purpose timer (PTM)
 - Two Periodic Interrupt Timer (PIT)
 - IEEE 1588 Timers (part of Ethernet Subsystem)
- Analog
 - 1x 12-bit 1.8 V SAR ADC with self-test
- Communications
 - UARTw (LIN, I1)
 - Serial peripheral interface (SPI)
 - I2C blocks
 - PCI express 2.0 with endpoint and root complex support
 - L-FAST serial link
 - GbE Ethernet with PTP IEEE 1588
 - FD-CAN
 - FlexRay Dual Channel, Version 2.1 RevA

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

NXP

4.7 PCB routing guidelines

DDR3/DDR3L PCB design

• CLK/Address/Commands

- Route with 50 ohm controlled impedance and differential pair (CLK) with 100 ohm controlled impedance
- Use Fly by topology in case of multiple memory components
- Address and command lines Terminated to VTT with 50 ohm
- To be referenced with Power, not Ground
- Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory; memory to memory as well
- All traces to be routed in internal layers
- Preference is to use only two layers for routing this group
- Limit the via number to less than three

S32

General

NOTE

The differential clock lines on the DDR3 interface should use AC termination scheme, with a 0.1 μ F series capacitor and referenced to DDR IO supply ($V_{DD_DDR_IO}$).

• Data/Strobe

- Route with 50 ohm controlled impedance and differential pair (DQS strobe) with 100 ohm controlled impedance
- Data to be routed within 33 mils with respect to respective strobe
- To be referenced with Ground
- All traces to be routed in internal layers
- Strictly to be routed in only two layers
- Avoid more than two vias

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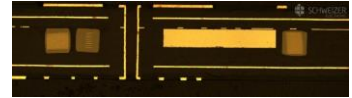
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Impedance Control

How to get a realistic Z_0 number?

- The definition of a proper impedance target for interconnects is rather old, validation is done via pcb grinding patterns and measurement
- Impedance = Ratio of current and voltage between two terminals of a circuit



Google impedance formula

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left(\frac{5.98H}{0.8W + T} \right) \times \left(1 - \frac{H_1 - T - H}{0.1} \right) \text{ ohms}$$

$$T_{pd} = 84.75 \times \sqrt{0.475 \times \epsilon_r \times \left(1 + e^{-1.55H_1/H} \right) + 0.67} \text{ psec/inch}$$

$$C_0 = \frac{T_{pd}}{Z_0} \text{ pF/inch}$$

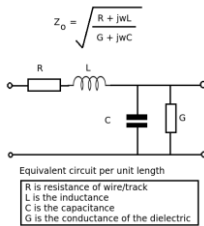
$$Z_0 = \frac{120\pi}{2.0 \sqrt{2.0 \pi \sqrt{\epsilon_r + 1.0}} \ln \left\{ 1.0 + \frac{4.0h}{W} \left[\frac{14.0 + 8.0/\epsilon_r \pi}{11.0} \right] \right.}$$

$$\left. + \sqrt{\left(\frac{14.0 + 8.0/\epsilon_r \pi}{11.0} \right)^2 \left(\frac{4.0h}{W} \right)^2 + \frac{1.0 + 1.0/\epsilon_r \pi}{2.0}} \right\}$$

Where $W' = W + AW'$

$$AW' = AW \left(\frac{1.0 + 1.0/\epsilon_r \pi}{2.0} \right)$$

$$AW = \frac{1}{2} \ln \left[\frac{4e}{(v/h)^2 \left(\frac{1/\pi}{w/h + 1.1} \right)^2} \right]$$



$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln \left(\frac{1.9(2H + T)}{(8W + T)} \right)$$

$$C_0 = \frac{5.55 \cdot 10^{-11} \epsilon_r}{\ln [3.81 H / (.8W + T)]}$$

$$t_{pd} = 3.34 \cdot 10^9 \sqrt{\epsilon_r}$$



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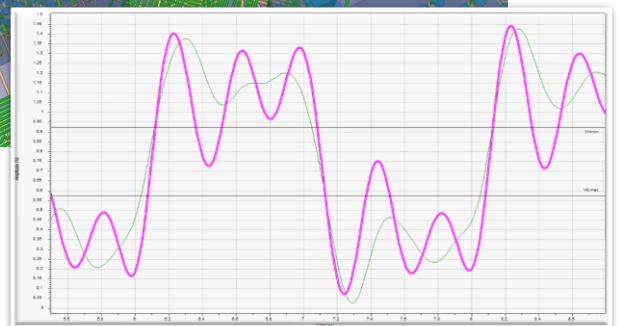
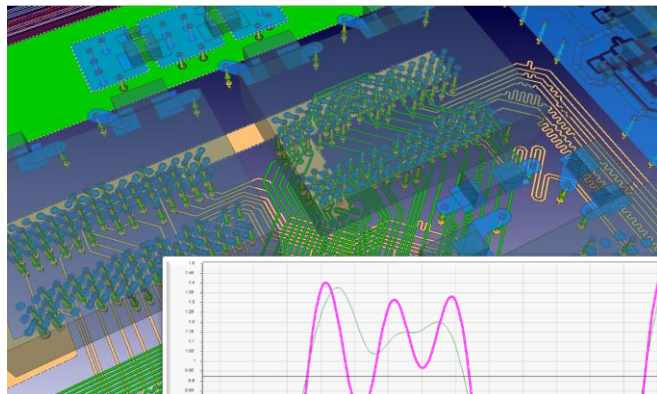
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Impedance Control – Impact of Violations

Signal Integrity Consequences

- Low Power DDR3 Signal with impedance requirement of 50 Ohm
- An in-depth impedance and SI simulations regarding tolerances did show that 60 Ohm (tolerance +20%) will cause false switching (→ system operation on risk, ringback below threshold, timing error likely) while
- An optimal switching occurs between 42 and 49 Ohm



LP-DDR3 Adress-Signal 60 Ohm (magenta) and 42 Ohm (green), picture © TEWS GmbH

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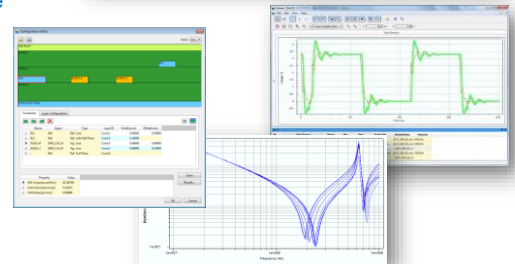
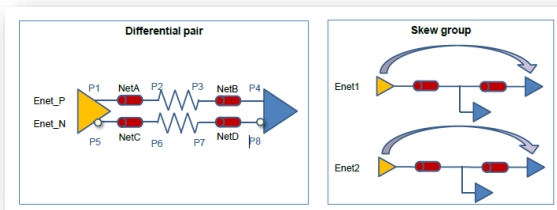
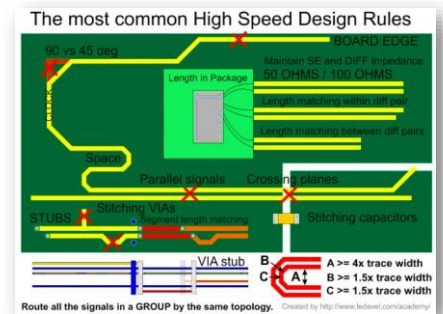
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High Speed Design & Signal Integrity

Coping a very Complex Problem Domain

- To support all relevant high speed speed requirements, the key high speed design features are:
 - (1) Impedance control
 - (2) Skew/length matching & topology control
 - (3) Rule Definition for High Speed routing (pin-pairs, impedance max-vias etc)
 - (4) Designing against these high speed rules
 - (5) What-if capabilities are needed (topology, terminations)
 - (6) Concurrent SI and PI analysis allows a immediate judgement of the electrical performance for design decisions



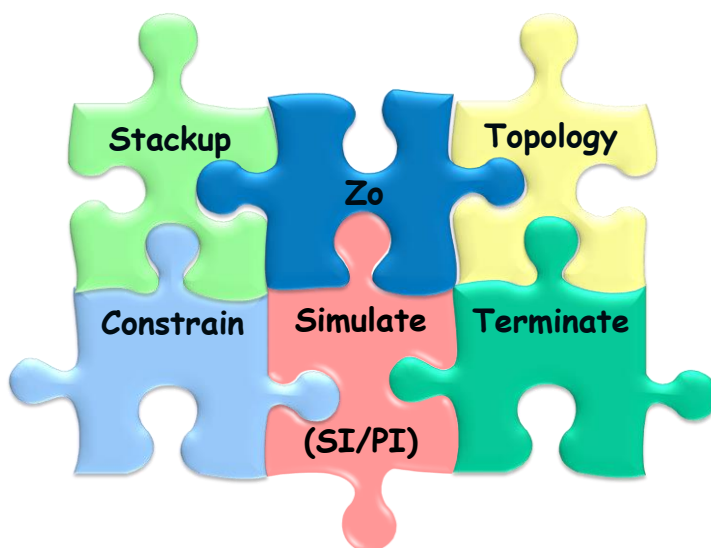
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The High Speed Design Puzzle



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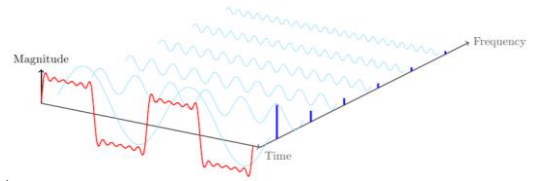
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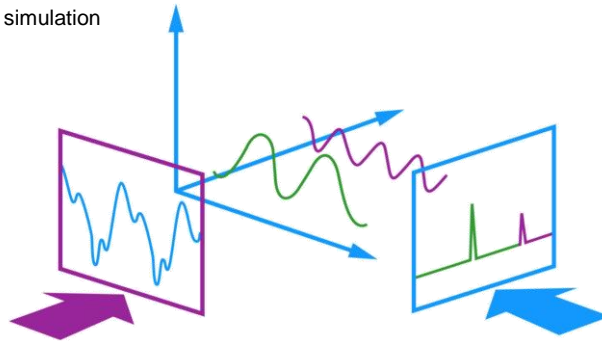
The SI Simulation Dilemma

Time Domain vs. Frequency Domain

- Frequency domain is more accurate for circuit analysis
 - But it's difficult to handle non-linear devices (most semiconductors)
- Time domain is more accurate for non-linear devices
 - But circuit behaviour is frequency-dependent
- The faster the circuit, the more frequency-domain effects dominate
 - Some constants at lower frequencies become variables at higher frequencies
- As a consequence, Zuken CR-8000 includes both, a time domain simulation engine and a frequency domain simulator



Time Domain Frequency Domain



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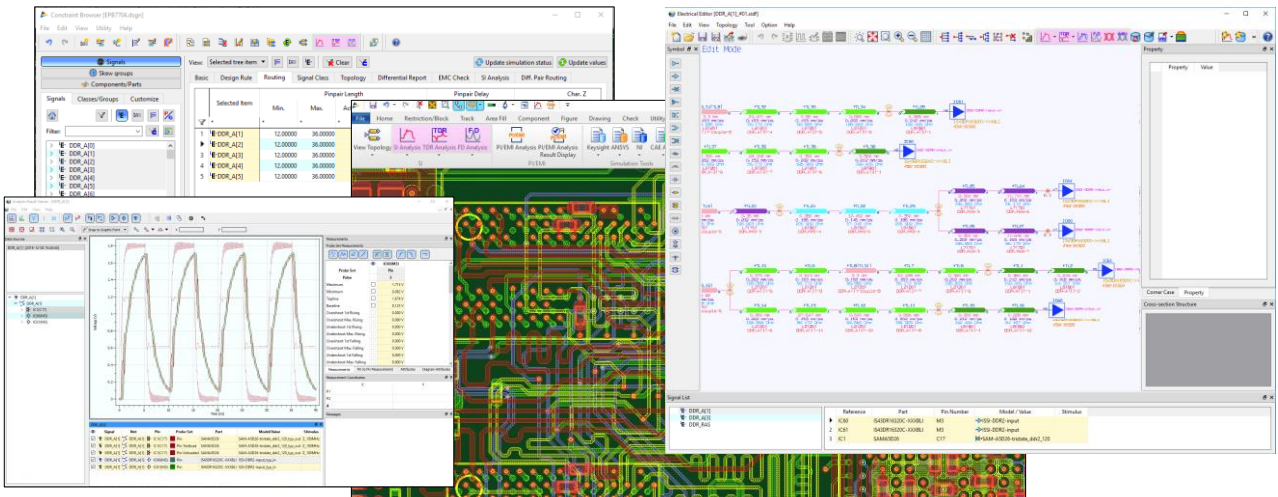
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Concurrent Signal Integrity

Direct Integration within PCB-Design-Process – SI on a Single Mouseclick

- Simulate from within place and route process concurrently or launch simulation from a Constraint Management tool (Spreadsheet) or create snapshots for sandbox investigations and parametric studies



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Simulation means Model-Building

Shared Task between User and ECAD System

Discretes:

Scalar value from CAD library or if parasitics to be modelled in SPICE or as Blackbox S-Parameters

Vias:

Complex lumped circuit (π element automatically computed by the EDA tool)

Alternative: Blackbox S-Parameters from 3D solver or measurement

Active Components (ICs):

Vendor supplied IBIS models (or IBIS-AMI in case of SERDES)
Can include package model (as RLC or S-Parameter)

Seldom SPICE (require then typically decryption key from IC vendor)

Transmission Lines:

Characterized by an TL model (lossy), simplified as Z_0 and t_d

Computed by a field solver (part of SI/EDA tool, automatically, can be parametrized)

Single ended or coupled

Alternative: Blackbox S-Parameters

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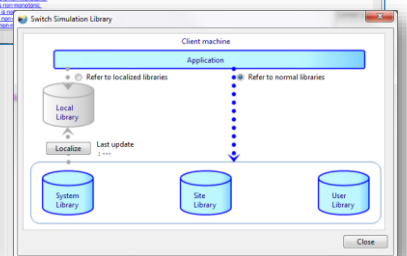
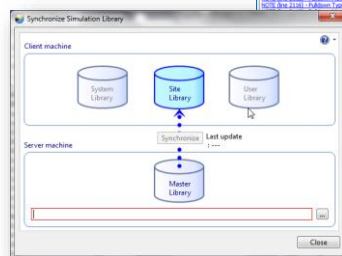
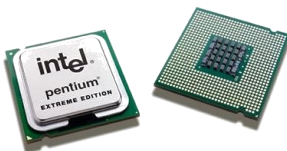
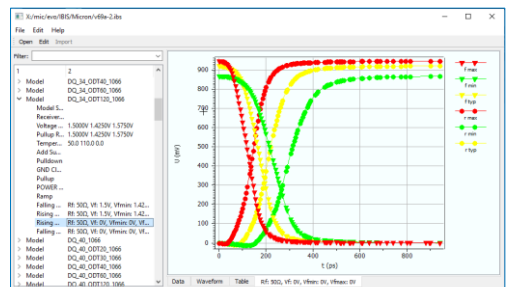
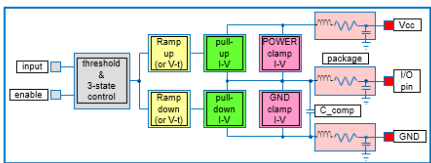
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Simulation Models ('Modelling Pain ?')

- IBIS is in place as SI modelling standard since 1993 (now Rev 7 in standardization)
- Supported by all major SI simulation tools
- CR-8000 simulation bases on a Simulation Library (SLM) which the user can populate with IBIS (or SPICE) models
- Various library hierarchies exist (e.g. user/project/company wide)
- Synchronisation with company wide master library possible



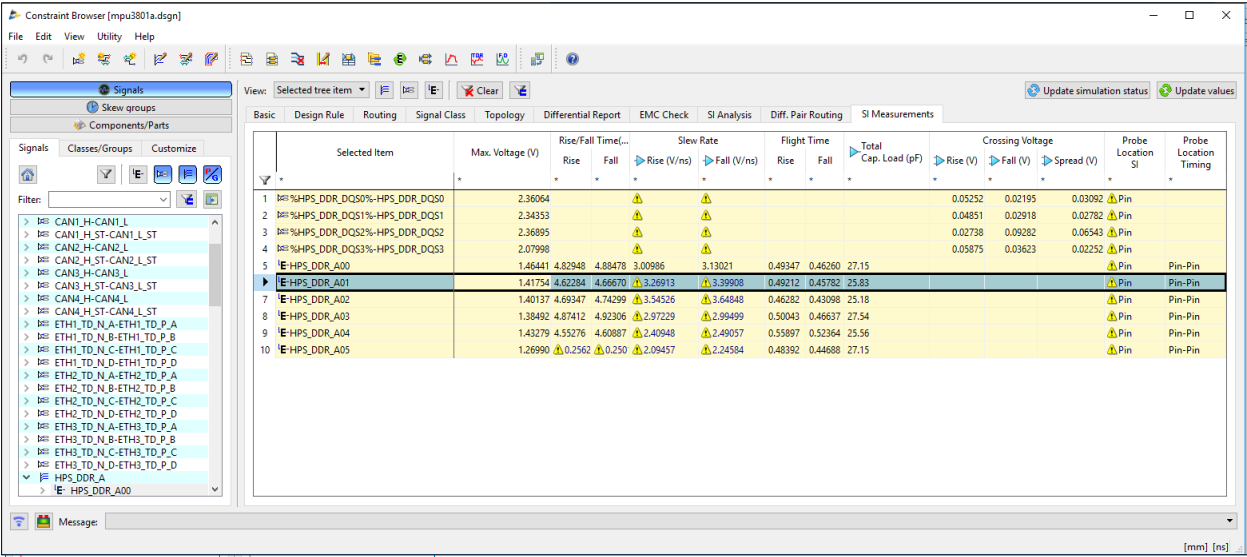
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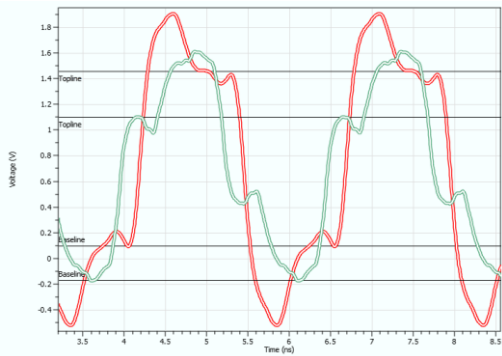
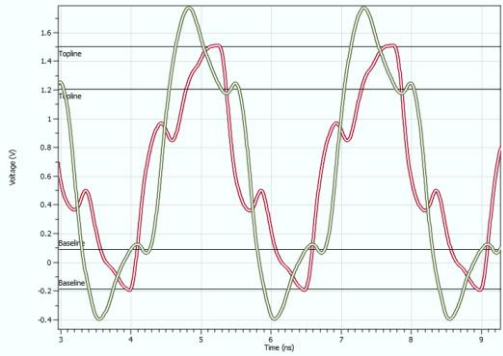
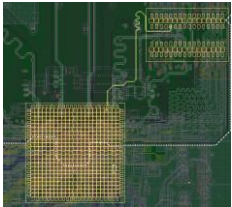
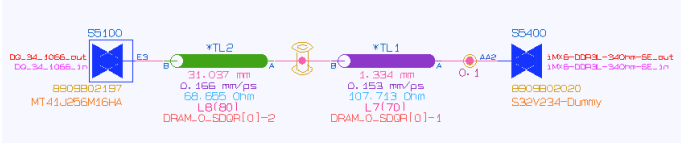
Signal Integrity – Batch Analysis Reduces Problem Space
Minimize Interactive Analysis Runs



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Signal Integrity – Reflection and Impedance
DRAM_DQR[0] – 400MHz – Read & Write

- Reflection due to impedance discontinuity



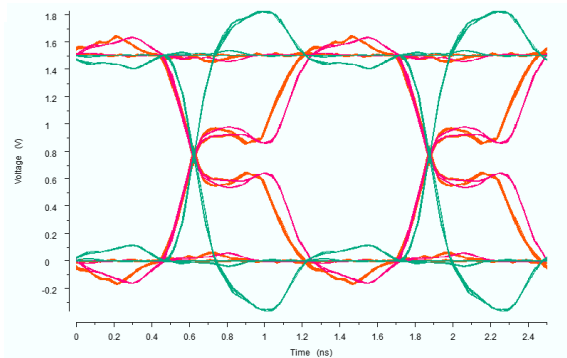
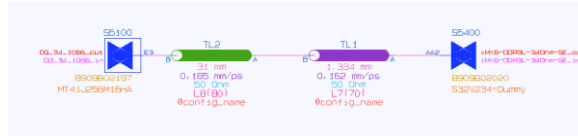
CPU: Write Memory: Read CPU: Read Memory: Write

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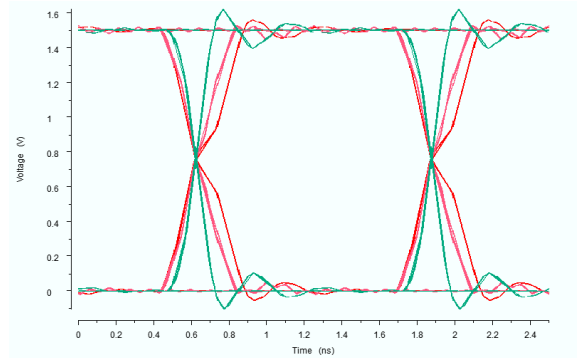
Signal Integrity – Reflection and Impedance

DRAM_DQR[0] – 400MHz – Read & Write

- Removal of impedance discontinuity (sandbox)



Original



Modified

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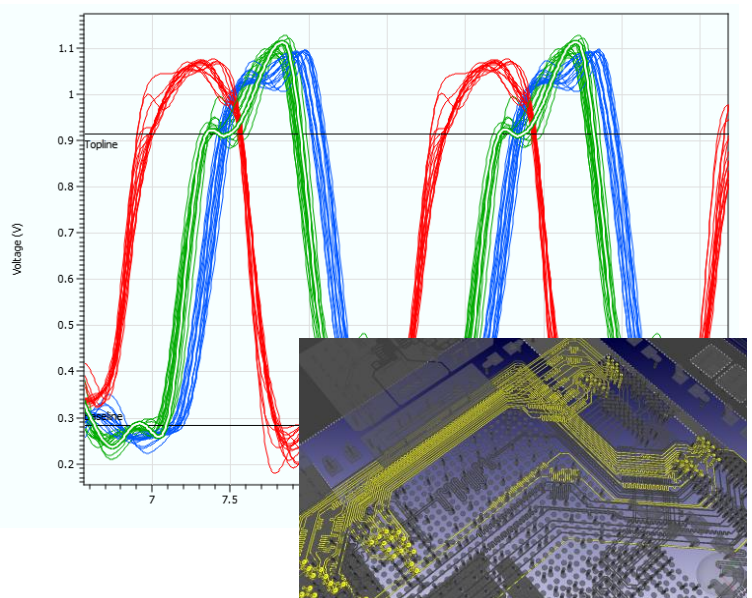
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Signal Integrity – Skew in DDR Addresses

Micron DR4 – 400MHz

- NXP iMX6 & Micron memory, fly-by topology
- Whole DDR address bus
- 400 MHz, speedgrade: 1066
- Simulation result (here pin waveforms only, DIE waveforms turned off for clearness of diagram) shows significant skew at the receivers within the address bus (→ violation of IC vendor requirement/constraint ?)
- Simulation time: less than 2 mins (parallel simulation)

ID	Task	Duration (s)	Priority
7969	DRAM_0_ADDR[0]_02 (04%)	4	High
14188	DRAM_0_ADDR[0]_02 (04%)	4	High
6400	DRAM_0_ADDR[0]_02 (04%)	4	High
9472	DRAM_0_ADDR[0]_02 (04%)	4	High
16276	DRAM_0_ADDR[0]_02 (04%)	2	Low
11368	DRAM_0_ADDR[0]_02 (04%)	0	Low
6800	DRAM_0_ADDR[0]_02 (04%)	0	Low
7256	DRAM_0_ADDR[0]_02 (04%)	1	Low



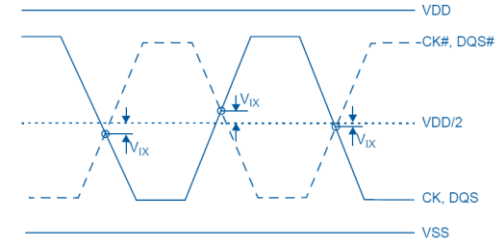
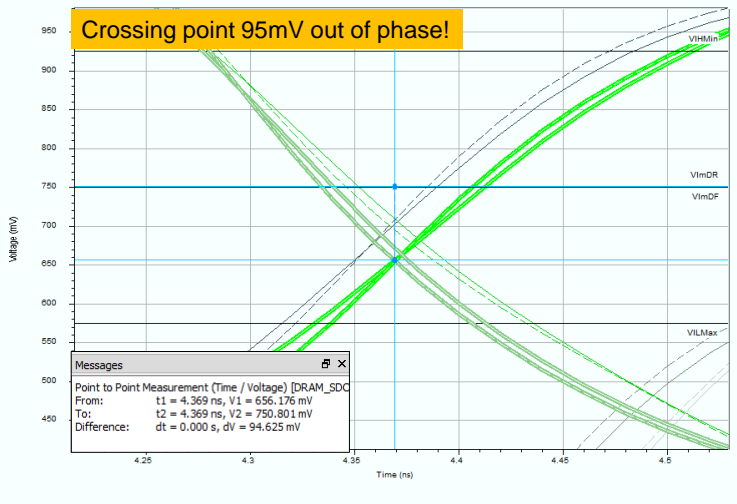
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Signal Integrity – JEDEC Compliance
Differential Crossing Point DDR3

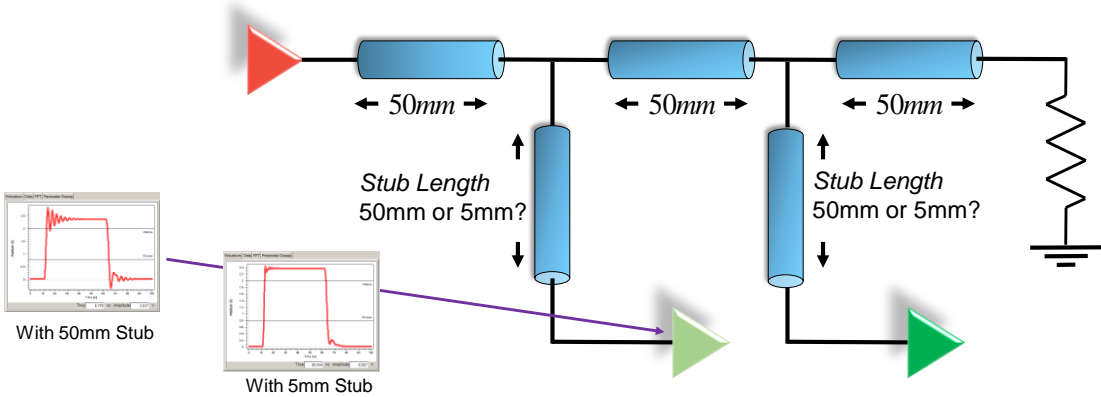


Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit
		Min	Max	
V _{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV
V _{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-175	175	mV



Signal Integrity - Parametric Studies
Stub Length and Waveform Integrity

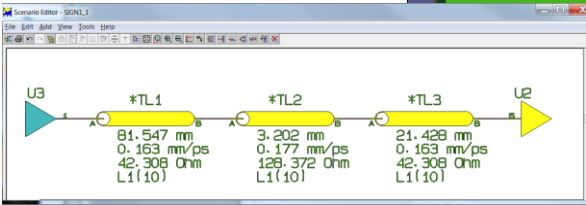
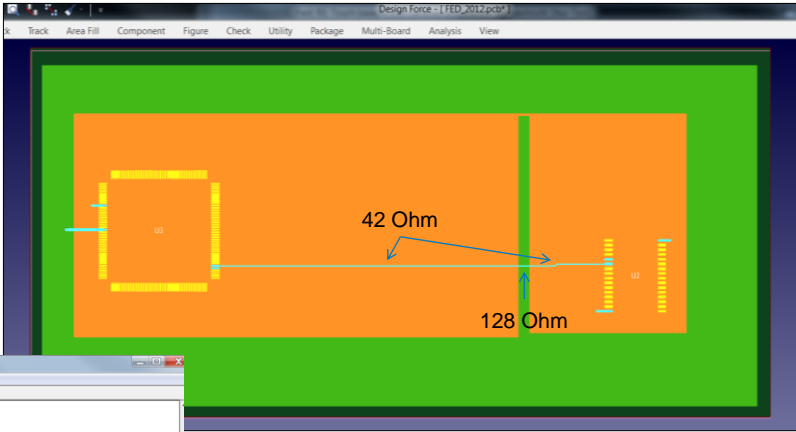
- In a **Daisy Chain** topology, *stub lengths* should be very short (IC vendor requirement), but routing often requires to have a stub to route into an IC
- Long stubs make signals reflect from transmission line junctions
- Shorter *stub lengths* are needed for faster *rise times* (e.G. DDRx)



SI & EMC Guidelines at PCB Level
High-Speed Nets crossing a Gap



- EMC issue (parasitic antenna) and SI issue (reflection due to impedance mismatch), but timing as well
- Forensic study on a DDR3 signal

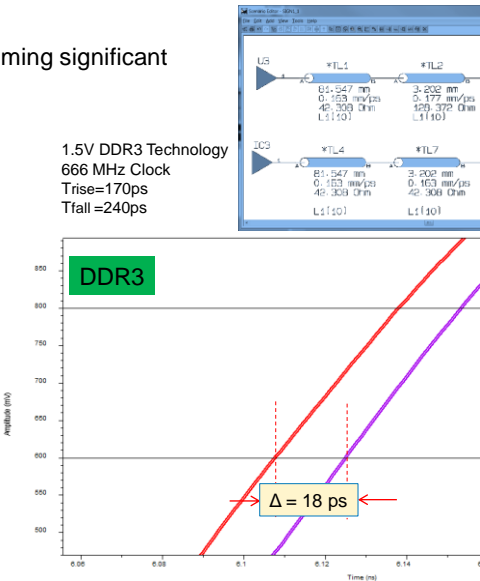


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SI & EMC Guidelines
High Speed Nets crossing a Gap



- Impact on signal timing significant
- Skew constraint ?



XILINX

Chapter 5: Processing System (PS) Power and Signaling

The skew limits can be increased if the memory interface is not operated at the maximum frequency, and/or if a faster memory device is utilized. See [Appendix A, Processing System Memory Derating Tables](#) for derating tables for DDR3, DDR3L, and LPDDR2.

Table 5-9: DDR Delay Match

Signal Group	LPDDR2	DDR2	DDR3/3L
DQ/DM to DQS, P/N in data group	±10 ps	±20 ps	±10 ps
Address/Control to CK, P/N	±10 ps	±25 ps	±10 ps

Route the CK traces to be equal to or longer than the DQS traces per byte lane. This is necessary because:

- The write leveling is capable of adjusting the clock to write DQS alignment over a wide range, assuming the clock trace length is longer than the DQS traces.
- The read leveling is capable of adjusting the read data eye to read DQS over a wide range. The adjustment is per byte, so board skew between bits (DQ,DM) should be minimized, as indicated in Table 5-9.
- There is no automatic training for aligning command/address to clock, but a fixed offset is programmable and can be used if necessary. Skew between CK and address/control should be minimized, as indicated in Table 5-9.

DDR Trace Impedance

All DDR signals except DDR_DRST_B require controlled impedance. DDR_CKE also requires controlled impedance in DDR3/3L. Table 5-10 shows the required trace impedance for DDR signals.

Table 5-10: DDR Trace Impedance

Signal Group	LPDDR2	DDR2	DDR3/3L	Comments
Single-ended	40Ω	50Ω	40Ω	±10% tolerance
Differential	80Ω	100Ω	80Ω	±10% tolerance

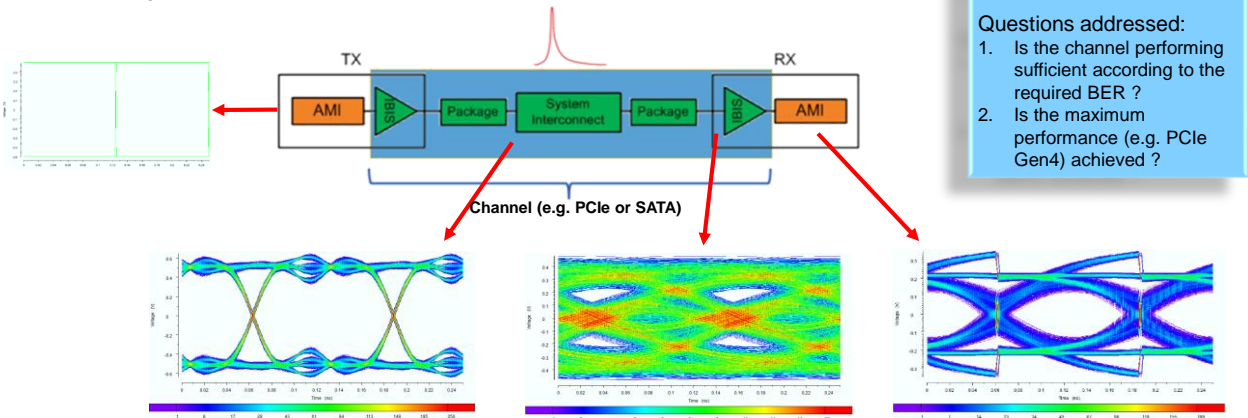
DDR3 and LPDDR2 memory also require an additional resistor connected to the ZQ pin to calibrate the device's output impedance. Table 5-11 shows the required RZQ values.

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Signal Integrity - SERDES Channel Analysis

Xilinx GTX Transceivers- Equalization Optimization

- Modern high data rate transceivers have to comply very tight BER targets (e.g. USB = 10^{-12})
- Transceiver silicon can be programmed to reconstruct the edges of the eye diagram (pre-emphasis and equalization)
- SERDES SI simulation allows to predict channel performance, BER and optimal settings of TX and RX



Opened eye due to equalization.

Questions addressed:

1. Is the channel performing sufficient according to the required BER ?
2. Is the maximum performance (e.g. PCIe Gen4) achieved ?

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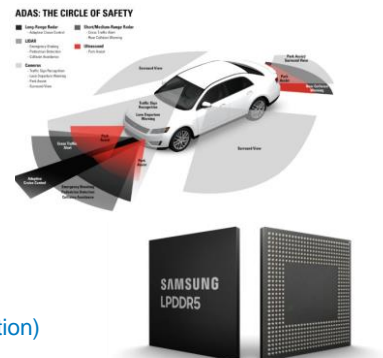
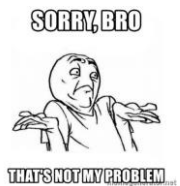
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Signal Integrity – Not my Problem ?

SERDES is a thrilling Technology

- You do not do PCIe, SATA or HDMI, so you assume SERDES and programmable devices are not on your 'design problems to come' roadmap?
- I seriously doubt that:
 - What about USB?
 - Do you do automotive? How do you expect ADAS (and other things like LIDAR, MIPI etc) to be realized?
 - There is an Automotive SERDES Alliance (ASA) since 2019
 - Ethernet and bus-systems will be in the cars of the future



- New memory generations (DDR5) will use programmable techniques (equalization) to realize high data rates, same kind of problems

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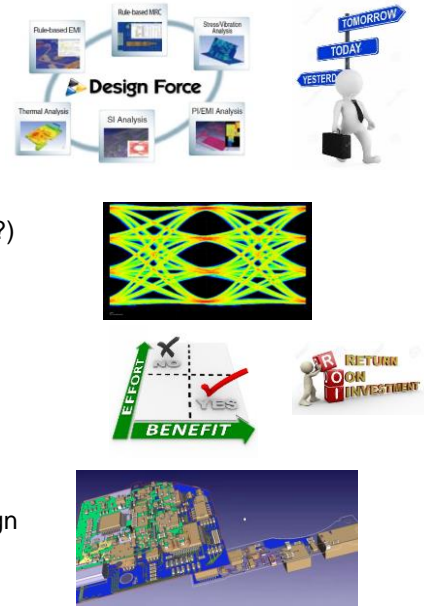
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Recap: Where are we today with PCB-Design ?

- PCB design becomes seriously complex for many application domains (not all)
- PCB related analysis is state of the art to a more or less extend (SI, PI, EMI, thermal), analysis should be an integral part of PCB design tool (integration rather than interfaced → 'concurrent analysis')
- Design problems further increase (someone heard about Moore law?)
→ analysis tools must cope with this and will do (there are no rectangular shapes anymore – in fact, they never did exist). Now we have things like 56Gbs links with PAM4 encoding as shown at the right.
- A smooth and easy to use process flow is key for success, then analysis tools do 'pay back' !
- PCB CAD process leaves the border of two dimensions (3D design, hence, 3D manipulation of copper and components, not just 3D visualization) and the single board domain (→ Multiboard PCB Design & Analysis)



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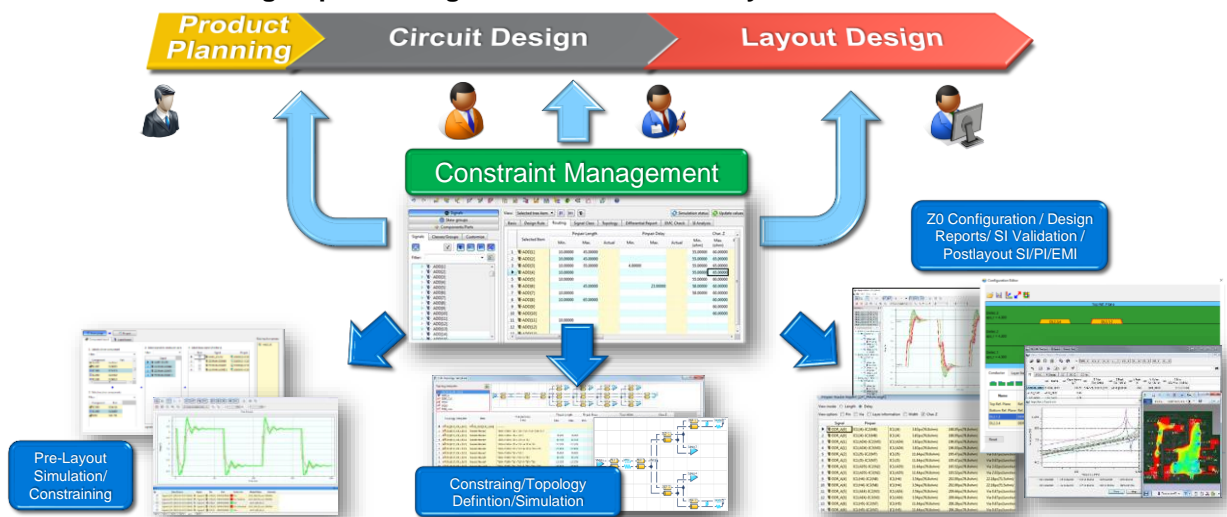
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High-Speed Design Overview Complete Design Process Solution

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High Speed Design and Concurrent Analysis for SI&PI



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ZUKEN®**Conclusion**

Signal Integrity and EMC are major design issues for PCB designers these days with importance increasing on a daily base



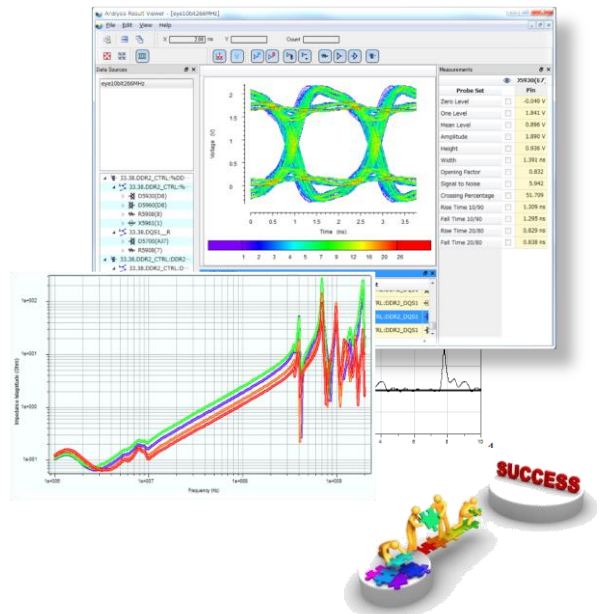
Problems should be avoided by a proper design process with SI and EMC in mind (rather than post-layout detection and fault fixing)



Technology is available (and in use) which is proven to be very accurate and efficient – virtual prototyping and working on a digital twin gains acceptance here.



Zuken CR-8000 offers a design process for high speed boards with concurrent analysis to design for Signal Integrity, Power Integrity and EMC compliance (as other EDA tools do)



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Need Help? ZUKEN EDA Services

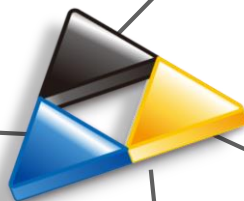
Solutions beyond Software

**ZUKEN®**

Find the (high-speed) problems before the problems find you!

**Training & Education**

- EMC compliant PCB Design
- Signal Integrity for PCB Designers
- Power Integrity for PCB Designers
- Simulation methods and models for SI/PI/EMC
 - IBIS Models, SPICE Models, S-Parameters
 - Numerical methods, time/frequency domain
- Introduction into EMC, SI and PI for managers and team-leaders

**IBIS Library Support****Custom Workshops**

- Customized tool training using your own design(s)
- Tool introduction support and process flow changes
- Analysis workshops
- High speed design methodology workshops
- Design for EMC

Design Support

- Design Reviews
 - SI, PI, EMC
 - EMC-Adviser DRCs
- Simulation Support
 - Reflection, Crosstalk, margins, PI, IR-Drop
 - ZUKEN simulators and 3rd party (e.g. HSPICE)
- Design optimization
- Eye Diagram analysis
- Constraining



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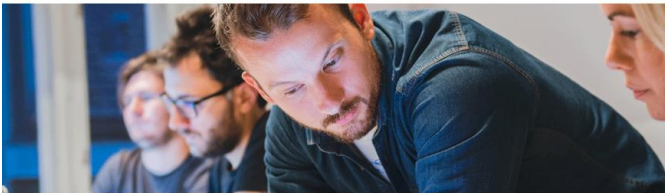
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Interested in a more detailed Follow-up?
One Day Seminar (Experience Day) on Signal Integrity – on request (Zuken inhouse or onsite)



Zuken Experience Day: Signal-Integrität und
Eigenstörsicherheit elektrischer Baugruppen

Zuken Trainingszentrum Am Söldnermoos 17, 85399 Hallbergmoos

beschränkte Plätze

Machen Sie sich ein Bild vom Stand moderner Entwicklungswerkzeuge zur Sicherstellung der Signal-Integrität und Eigenstörsicherheit elektrischer Baugruppen. Mit diesem Zuken Experience Day bietet Zuken kompakte Hands-on Workshops an, in denen Interessierten die Möglichkeit erhalten, sich unter Anleitung von Experten ein Bild von dem Arbeiten mit den aktuellen Releases unserer Software-Tools zu machen.

Vorname:

Nachname:

Email Adresse:

Inhalt – Zuken Experience Day

- Signal- und Power-Integrität und EMV-gerechtes Design
- Aufstellen und Umsetzung von Design-Regeln
- Modernes Constraint Management
- Erstellen von Szenarien
- Einsatz von Simulationsmodellen
- Anwendung eines SI-Simulators

Thank you for attending!

No one believes in simulation results except the guy doing the simulation ...

Everyone believes in measurement results, except the guy doing the measurements !!!

(Source unknown)

The Partner For Success