

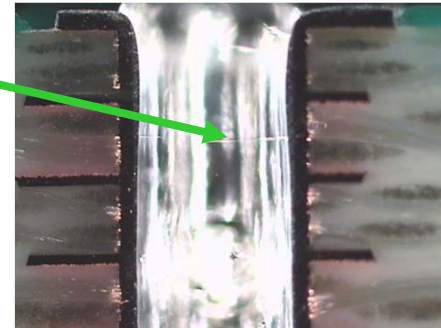
# Recommended values “Solder resist design for vias“

(The recommended values are not legally binding and the layout prescriptions are subject to an application-specific evaluation)

## Objective:

- No undefined conditions, no exposed copper in vias due to resist residues
- Completely metallised/coated surface on pads and in via barrels
- Scope: photoimageable solder resist, all solder surfaces

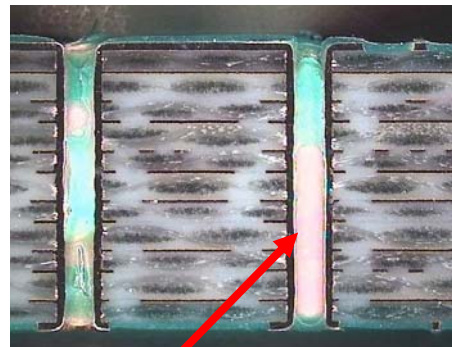
Objective



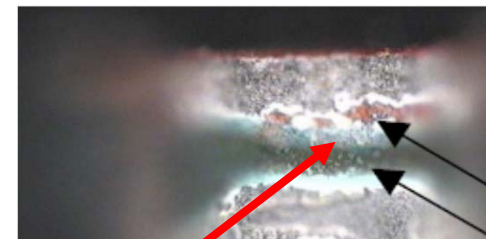
## Defects



exposed Cu in barrel,  
resist residues in hole



exposed Cu in barrel,  
resist residues in hole



# Recommended values “Solder resist design for vias”

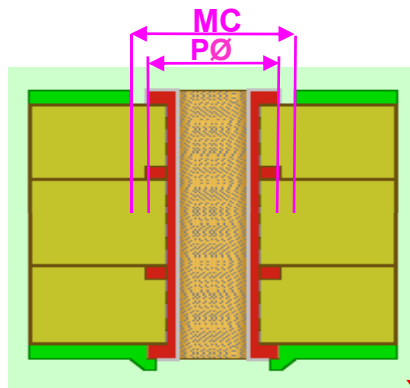
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## Methods to reach the objectives:

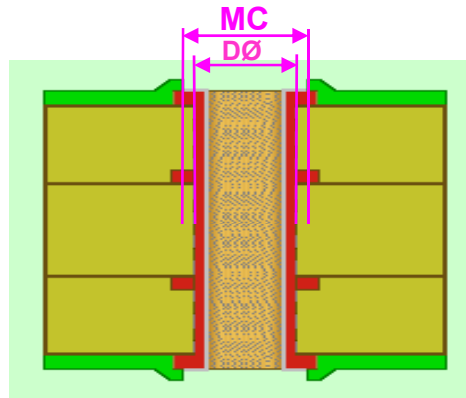
- Clearance of vias from solder resist
- Sufficient clearance from solder resist and development of vias and pads

## Recommended parameters:

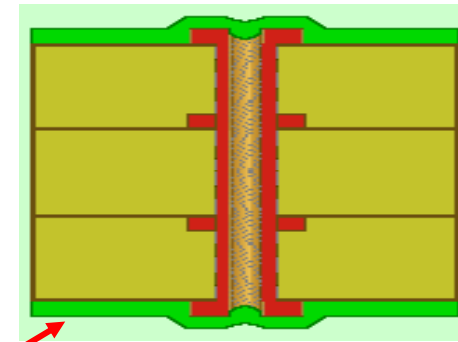
Mask clearance = MC  
Pad diameter + 0.1mm



Mask clearance = MC  
Drill diameter + 0.15 mm



No mask clearance single/ double-sided  
or  $\leq$  drill diameter + 0.15 mm



Preferred, process-safe for  
drill diameter  $\geq 0.3$  mm,  
typical aspect ratio 1:5

Risk of air inclusion, exposed copper,  
residual chemicals, burst:  
⇒ no warranty through PCB manufacturer  
⇒ Alternatives on foil 3

# Recommended values “Solder resist design for vias”

(The recommended values are not legally binding and the layout prescriptions are subject to an application-specific evaluation)

## Objective:

- No solder penetration through plated vias, for example under QFP, BGA
- Isolation of BGA pads from via, development of solder dam to prevent solder outflow

Alternative methods (additional expense), if clearance according to foil 2 is impossible:

- A Hole filling print on wave solder side of PCB
- B Trimming of solder resist, providing solder resist bridge from pad to via
- C Complete plugging

